AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (CURRENTLY AMENDED) A circuit comprising:

a register stack configured as (i) a plurality of segments addressable through a segment address signal and (ii) a plurality of registers within each of said plurality of segments, said plurality of registers being addressable through a register address signal; ~~and~~

a control circuit connected to said register stack and configured to (i) store a plurality of register states, (ii) store a segment count signal, and (iii) present said segment address signal responsive to said ~~plurality of~~ register states, said segment count signal, and said register address signal; and

a state register connected to said control circuit and configured to present said register states to said control circuit, wherein each of said register states has one associated register of said registers.

2. (CURRENTLY AMENDED) The circuit according to claim 1, wherein at least one of said register states is fixed in a global state indicating that data cannot be pushed onto said one associated register.

3. (CURRENTLY AMENDED) The circuit according to claim 1, wherein at least one of said register states is fixed in a

stackable state indicating that data can be pushed onto said one associated register.

4. (PREVIOUSLY PRESENTED) The circuit according to claim 1, wherein said register stack further comprises:

a first portion disposed within a processor and configured as at least one segment of said plurality of segments; and

a second portion disposed external to said processor and configured as at least one segment of said plurality of segments.

5. (CURRENTLY AMENDED) The circuit according to claim 1, wherein said control circuit comprises:

a status circuit configured to present a gating signal responsive to both said register address signal and said register states.

6. (CURRENTLY AMENDED) The circuit according to claim 5, wherein said status circuit comprises:

a comparator configured to present said gating signal ~~responsive to~~ by comparing said ~~plurality of~~ register states and said register address signal.

7. (CURRENTLY AMENDED) The circuit according to claim 5, wherein said status circuit comprises:

a memory device configured to (i) store said ~~plurality of~~ register states and (ii) present said gating signal ~~responsive to~~ by reading out one of said ~~plurality of~~ register states ~~and~~ as addressed by said register address signal.

8. (PREVIOUSLY PRESENTED) The circuit according to claim 17, wherein said plurality of logic gates are further configured to present said segment address signal as a predetermined address responsive to said gating signal having a global state.

9. (CURRENTLY AMENDED) The circuit according to claim 8, wherein said status circuit comprises:

a comparator configured to present said gating signal ~~responsive to~~ by comparing said ~~plurality of~~ register states and said register address signal.

10. (CURRENTLY AMENDED) A method of controlling a register stack comprising the steps of:

(A) comparing a register address with a plurality of register states to present a gating signal;

(B) gating a segment count with said gating signal to present a segment address; ~~and~~

(C) addressing a plurality of segments within said register stack with ~~said register address and~~ said segment address; and

(D) addressing said registers within one of said segments with said register address.

11. (ORIGINAL) The method according to claim 10, wherein step (A) further comprises the sub-steps of:

presenting a signal communicating said plurality of register states; and

selecting one of said plurality of register states as said gating signal based upon said register address.

12. (CURRENTLY AMENDED) The method according to claim 10, further comprising the step of:

~~setting~~ writing said plurality of register states into a register under software control in response to a reset handler operation for a processor executing said software.

13. (ORIGINAL) The method according to claim 10, further comprising the step of:

incrementing said segment address in response to a push instruction.

14. (ORIGINAL) The method according to claim 13, further comprising the step of:

decrementing said segment address in response to a pop instruction.

15. (CURRENTLY AMENDED) A circuit comprising:

~~means for storing a~~ register stack means configured as (i) a plurality of segments addressable through a segment address and (ii) a plurality of registers within each of said plurality of segments, said plurality of registers being addressable through a register address;

means for storing a plurality of register states;

means for storing a segment count; ~~and~~

means for presenting said segment address responsive to said register address and said plurality of register states and said segment count; and

means for present said register states to said means for storing, wherein each of said register states has one associated register of said registers.

16. (PREVIOUSLY PRESENTED) The circuit according to claim 1, wherein said control circuit comprises:

a counter configured to present said segment count signal identifying a current segment of said segments at a logical top of said register stack.

17. (CURRENTLY AMENDED) The circuit according to claim 5, wherein said control circuit further comprises:

a plurality of logic gates configured to present said segment address signal ~~responsive to~~ by logically ANDing said gating signal and said segment count signal.

18. (PREVIOUSLY PRESENTED) The method according to claim 10, further comprising the step of:

presenting said segment address as a predetermined address responsive to said gating signal having a global state.

19. (CURRENTLY AMENDED) The method according to claim 10, comprises the step of:

transferring ~~storing~~ said register states from a first memory to a second memory prior to said comparing.

20. (PREVIOUSLY PRESENTED) The method according to claim 10, further comprising the step of:

storing said segment count prior to said gating.